Spring 2005: ENTC 249
Digital Logic Circuits: Rapid Digital System Design

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CLASS SCHEDULE

- LECTURE: Fermier 110
- MWF 3:00pm – 3:50pm
- LAB: Thompson Hall 011
- EXAMS: Exam 1 – Feb. 04* (Friday)
- Exam 2 – Mar. 04* (Friday)
- Final Exam – May. 10* (Tuesday) from 1:00pm – 3:00pm

***This syllabus contains a tentative course schedule. The policies and dates stated within are subject to change at the discretion of the Professor.**

COURSE DESCRIPTION

This course is an advanced class for learning digital systems including microprocessors. Contemporary digital system design methodology, hardware description languages (i.e., VHDL and Verilog), FPGA-based design platform, and related system-level digital design issues are covered in the class.
A FPGA-based platform is used for implementing and verifying a microprocessor-based digital system including parallel and serial (UART) data communications in the laboratory.

COURSE EMPHASIS

The four stages pipelined RISC processor architecture, named JJ249-04, is introduced. As a part of designing the processor, students will learn about digital logic including combinational and sequential logic and other digital logic systems. In addition, a microprocessor synthesizable soft-core will be implemented and verified with FPGA-based hardware development tool including both simulation and synthesis.

PROCEDURE

The class will consist of lectures, laboratory project work, and other assignments. Problems and reading will be assigned. It is the responsibility of the student to stay current with assignments and project work.

PREREQUISITES

ENTC 219 or higher. You must meet the course prerequisites to enroll in this course. Failure to fully meet these prerequisites will result in failure in this class.

TEXTBOOK

Rapid Prototyping of Digital Systems: 2nd Edition, J. Hamblen and M. Furman, Kluwer Academic Publishers

REFERENCE

- Logic and Computer Design Fundamentals: 3rd Edition, Mano, M. Morris & Kime, Charles R.
- Computer Architecture: A Quantitative Approach: 2nd Edition, J. Hennessy and D. Patterson
- From time to time, reference materials will be made available to students. Generally, these will be placed on the ETID ftp server and course web page. The availability of these reference materials will be announced during lecture and/or laboratory sessions.

FTP SERVER & COURSE WEB PAGE

Course materials, including this syllabus, will be posted in the ENTC 249 directory on the ETID ftp server and course web page. It may be accessed through ftp://entc.tamu.edu/entc249 and http://etidweb.tamu.edu/classes/entc249. These sites should be checked periodically for new postings.

PARTS AND SUPPLIES

1. Each student is required to maintain an engineering journal.
2. Students are responsible for supplying their own prototype board, and additional parts for lab. The parts may be purchased anywhere, but the IEEE TECH parts store is recommended.
3. **Two 3.5", 1.44MB Floppy Disks and/or two 100MB Zip Disks**. You should always have a backup disk that contains an updated copy of all of your work. No consideration will be given to students based on an "I lost everything on my disk" excuse!!!!!!!

STUDENT EVALUATIONS

The student's course grade will be based on laboratory exercises, weekly engineering meetings, exams, and participation. The final grade will be computed approximately as follows:

- Tests (2): 20%
- Take-home tests & classroom-quizzes: 10%
- Labs: 25%
- Final Project: 20%
- Final Exam: 15%
- Participation: 10%

Course participation includes attendance, homework, quizzes, involvement in class and laboratory discussions and activities. The concepts presented in this course require substantial study and experience. Students will be provided homework exercises, reading assignments, laboratory problems, and additional work in order to develop this experience. Each student will be responsible for completing all assigned material, even if the work is not collected for grading. The Professor may choose not to grade submitted work that is disorganized or difficult to read.

ATTENDANCE

Class and laboratory attendance is mandatory. At the discretion of the Professor, roll will be taken at the beginning of each lecture and laboratory. Three late arrivals are equivalent to one absence. Only documented university approved absences from lectures will be allowed. Absences from the laboratory are addressed below.

Each student is responsible for all material presented during lectures and laboratory sessions. All work to be submitted (incl. homework, quizzes, laboratory reports, etc) must be submitted at the beginning of class or laboratory on the due date. Late work will not be accepted without either a valid university approved excuse (in which case the Professor will set the submission deadline, on a case-by-case basis) or a prior consent from the Professor. The laboratory teaching assistant does not have the authority to excuse a late assignment or an absence.

EXAMINATIONS

There will be four in-class exams, including the final exam. Tentative dates for the exams are included in this syllabus but are subject to change. Actual exam dates will be announced in class. The final exam will be given at the time specified by the university. Make up exams are not given unless permission is obtained from the Professor prior to the exam day or a valid, documented emergency has arisen. There may also be announced and unannounced quizzes. There will be no make up quizzes. Exams and quizzes will require a #2 pencil. Content will be taken from class lectures, homework, course text, handouts, and laboratory exercises (non-comprehensive listing).

Exams will be graded and returned to the student as quickly as possible. Every attempt will be made to grade exams within two weeks after the exam date. Once returned, graded exams should not be modified in any way. This includes writing notes, corrections, etc. When a graded exam has been modified, the Professor may choose not to accept it for re-grade consideration or any other purpose.

Exams will not be re-graded in the presence of the student, with one exception. If the student feels that an arithmetic error has been made, they may discuss it with the Professor at any time. Otherwise, if the student believes that they should have received more credit on an exam question, they may request reconsideration in writing. To do this, the entire original exam must be submitted, along with an explanation of why the grade should be raised, and what a fair grade would be. Of course, the instructor reserves the right to re-grade the entire exam.

ENGINEERING JOURNAL

Each student is required to maintain an engineering journal. The engineering journal will be brought to every lecture and laboratory session and can be reviewed by the Professor or laboratory teaching assistant at any time.

The engineering journal should be hardbound and contain numbered permanent pages (i.e., no loose pages). Students will use the journal to sequentially (i.e., no pages left blank) record the progress of all engineering (laboratory-related) work, specifications, designs, questions, test results, observations, references, contact information, etc. The journal should not be used for taking lecture notes, except when these pertain to engineering (laboratory exercise) assignments. Entries in the journal must be dated, with each new date beginning on a new page. The first page of the journal should include the student's name, course number, and section number.

LABORATORY

All laboratory work must be completed to meet the minimum requirements for a passing grade in the course. Laboratory work will include exercises, programs, and projects.

Students are required to notify the Professor and laboratory teaching assistant of any absence from the laboratory. The student has two weeks to makeup a missed laboratory. Students must request permission, in writing, from the Professor to makeup a missed laboratory. If permission is granted, the absences must be made up during "open lab" hours or a regularly scheduled laboratory. When making up a missed laboratory, the student will provide the teaching assistant a "Proof of Attending a Make Up Laboratory" form to complete. The completed form must be returned to the teaching assistant responsible for the student's laboratory section. Unexcused absences from the laboratory, which are made up, will result in a grade penalization of 15% for the missed lab. No grade penalty will be assessed for excused absences that are made up.

***** If a missed laboratory, excused or unexcused, is not made up within two weeks, the student will receive a grade of zero for that lab.**

***A lab session sign in sheet will be provided at the beginning of each lab.

***** Failure to sign in will result in an absence. Tardiness to labs by more than 10 minutes (determined by the laboratory teaching assistant) will be considered as an absence and must be made up.**

*** Students are expected to actively participate in the entire lab session. Leaving the lab prior to being dismissed by the laboratory teaching assistant will result in the student being counted absent.

The student is expected to read the current lab assignment and to prepare a pre-lab before coming to class. The prelab should include all necessary calculations, program block diagrams, program flow diagrams, pseudo code, etc. Pre-lab work will be due at the beginning of class. A lab write-up will be due at the beginning of the assigned due date. The lab write up will consist of a cover sheet, lab report, pre-lab (checked by the lab teaching assistant), and any additional required information (as indicated by the lab handout). The lab report must be typed and consist of an objective, specifications, design, implementation, test results, and conclusion. A suggested report format is provided in the Laboratory Syllabus, which is available on the course ftp site.

IMPORTANT

To Pass the course you must take all test, participate in and complete all lab assignments, submit all pre-labs and lab reports and have a lab passing grade of 60% or higher. Lab reports will be graded both on technical content and accuracy as well as correct grammar, punctuation, and spelling. It is recommend that you have someone else proofread your lab report before submitting it for grading. Circuit diagrams and other graphics must be professional quality and computer generated.

ACADEMIC INTEGRITY

The Texas A&M Honor Code will apply in this class. Academic integrity is of uppermost importance in your work. Each student must do his/her own work and give appropriate credit when the ideas or material of others is used.

Plagiarism of any kind is unacceptable, and will result in a failing grade in the course. Cheating on exams will, of course, have grave consequences. Exams will include an Honor Code Statement; failure to sign this statement may result in penalties and/or the exam not being graded.

This course will adhere to the 1996-97 Texas A&M University Regulations, Part I, Section 42. All students have the responsibility to be fully acquainted with and to comply with University Regulations. Every student should be familiar with the content of University Regulations regarding academic dishonesty.

The handouts used in this course are copyrighted. By "handouts," I mean all material generated for this class, which include but are not limited to syllabi, quizzes, exams, laboratory problems, in-class materials, and review sheets. Because these materials are copyrighted, you do not have the right to copy, unless I expressly grant permission.

AMERICANS WITH DISABILITIES ACT POLICY STATEMENT

The Americans with Disabilities Act (ADA) is a Federal anti-discrimination statute that provides comprehensive civil rights protection for persons with disabilities. Among other things, this legislation requires that all students with disabilities be guaranteed a learning environment that provides for reasonable accommodation of their disabilities. If you believe that you have disability requiring accommodation, please contact the Department of Student Life, Services for Students with Disabilities, in room 126 of the Koldus Building, or call 845-1637.

SUGGESTIONS

1. As a core element of the EET/TET curriculum, this course requires a great deal of your attention and concentrated study on a regular basis. Manage your time accordingly. It is generally accepted that university students study 2 hours for every hour of lecture and lab. The following is an estimate of study time (on a weekly basis) required by this course:
   - 3 hours – lecture
   - 6 hours – lecture study
   - 2 hours – laboratory
   - 4 hours – laboratory study/preparation

TOTAL = 15 hours per week.

2. To maximize the value of the lecture and laboratory experience, students are encouraged to read and study the related text material and to discuss these with peers, laboratory teaching assistants, and the Professor.

3. The student should make frequent practice of writing programs for the M68332 in order to gain a deep understanding of the course topics.

4. You may find the following web sites useful
   - http://eapo.tamu.edu/
   - http://www.tamu.edu/cae/
   - http://www.artsci.uc.edu/CollegeMain/cur_ug_students/study_tips.html

TENTATIVE LAB. SCHEDULE

Phase 1 - Introduction			
1st week	Introduction	(Verilog)	1 week
2nd week	Debounce/ Baud Rate Generator	(UP2/Compilation)	1 week
Phase 2 - Universal Asynchronous Receiver/Transmitter			
3rd week	Transmitter	(Functional Simulation)	1 week
4th	Receiver		1 week
5th	UART Integration	(Timing Simulation)	1 week
Phase 3 – Microprocessor (J249-05S)			
6th	Memory/FSM	(Individual work)	1 week
7th	Fetch	(Individual work)	1 week
8th	Decode	(team work)	1 week
9th	Execution	(team work)	1 week
10th	Memory-access	(team work)	1 week
11th	Integration	(group work)	1 week
12th	FPGA verification	(group work)	1 week
Phase 4 - Presentation			
13th	Final Documentation/presentation	(Individual/team/group)	1 week